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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/007,468	11/07/2001	Shinichi Shimomaki	01727/LH	2858

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EXAMINER	
JORGENSEN, LELAND R	

ART UNIT	PAPER NUMBER
2675	

DATE MAILED: 06/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/007,468	SHIMOMAKI, SHINICHI	
	Examiner	Art Unit	
	Leland R. Jorgensen	2675	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 24 May 2005 has been entered.

Claim Rejections - 35 USC § 103

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. Claims 1 – 9 and 11 - 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al, USPN 5,510,807, in view of Moon, USPN 5,825,343.

Claims 1 and 12. Lee et al. teaches a liquid crystal display device comprising a liquid crystal display panel [14] having a plurality of signal lines [column lines 24], a plurality of scanning lines,[26] and a plurality of display pixels [19] arrayed in a matrix and provided respectively near cross-points between the signal lines and the scanning lines through switching elements [20]. A driver supplies the plurality of signal lines [through column driver 16] with a display signal in a field period, and which scans [through row select driver 25] the plurality of scanning lines, to apply the display signal to the plurality of display pixels. Lee, col. 1, lines 20 – 55; col. 3, lines 13 – 40; and figure 1.

Lee teaches that the driver include means which supplies an initialization signal [precharge voltage V+ or V- during 6μs precharge time] including a single pulse voltage to the signal line [(i) or (j)], thereby applying the initialization signal to the display pixel, and thereafter supplies the display signal [(0~5V) or ((-5~0V) video signal during the video data banks periods #1 - #6] to the signal line and thereafter applying the display signal to the display pixel, at least one signal application period set within the field period. Lee, col. 5, line 62 – col. 6, line 33; col. 6, line 63 – col. 7, line 4; col. 7, lines 59 – 64; and figure 4.

Lee teaches that the scanning line [select scan line, N (k)] is one during both the precharge and the display signal time. Lee, col. 5, line 62 – col. 6, line 4; and figure 4 . Thus, Lee does not teach a first gate pulse and a second gate pulse.

Moon teaches a first gate pulse and a second gate pulse [two-pulse gate electrode voltage signals to each gate line]. Moon, col. 3, lines 46 – 55; col. 4, lines 50 – 58; col. 5, lines 21 - 25; and figures 5, and 7 – 9.

> As shown in FIG. 8, the gate electrode voltage pulse is twice applied to the gate lines of the liquid crystal pixels. The first gate electrode driving pulse precharges the liquid crystal capacitor C_{lc} and the grey voltage, which is applied to source terminal of the TFT-LCD is applied to the liquid crystal capacitor C_{lc} by the second driving pulse.

Moon, col. 4, lines 52 – 58.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the first and second gate pulse as taught by Moon with the liquid crystal display device as taught by Lee to improve a clear picture by double the duration of the driving voltage. Moon invites such combination by teaching,

> As described above, the present invention provides a driving device and a driving method for a TFT-LCD in which the liquid crystal pixels are correctly

> driven by applying a two-pulse gate electrode voltage which have the effect of doubling the duration of the driving pulse.

Moon, col. 5, lines 21 0 25. See also Moon, col. 1, lines 7 – 14; and col. 2, lines 24 – 58.

Claim 2. Lee teaches that the liquid crystal display panel includes a plurality of pixel electrodes arrayed in a matrix through the switching elements, and common electrodes opposed to the pixel electrodes, and the display pixels comprise the pixel electrodes, the common electrodes, and liquid crystal sandwiched between the pixel electrodes and the common electrodes. Lee, col. 3, lines 14 – 40; and figure 1.

Claim 3. Lee teaches that each of the switching elements of the liquid crystal display panel includes a thin film transistor. Lee, col. 1, lines 29 – 31.

Claims 4 and 13. Lee teaches that the driver applies the initialization signal voltage to the display pixels and thereafter applies the display signal after a predetermined hold time, in the signal application period in the field period, and the hold time is set to a time equal to or longer than a voltage-write response time of the display pixels. Lee, col. 6, lines 34 – 63.

Claims 5 and 14. Lee teaches that the initialization signal voltage in the driver has a value equal to or higher than a maximum voltage value of the display signal. Lee, col. 6, lines 54 – 62.

Claims 6 and 15. Lee teaches that the driver applies the initialization signal voltage and the display signal to the display pixels connected to the scanning lines of the liquid crystal display panel, at a predetermined time interval, sequentially for every one of the scanning lines, in the signal application period in the field period, and the time interval is set to a value at which timings of applying the initialization signal voltage and the display signal to every of the display

pixels connected to each of the scanning lines do not overlap each other. Lee, col. 1, lines 20 – 56; col. 3, lines 14 – 39.

Claims 7 and 16. Lee teaches that the application timing is set such that the driver applies the initialization signal voltage simultaneously to all the display pixels of the liquid crystal display panel, and thereafter applies the display signal to the display pixels connected to the scanning lines of the liquid crystal display panel, at a predetermined time interval, sequentially for every one of the scanning lines, in the signal application period in the field period. Lee, col. 5, line 62 – col. 6, line 33; and figure 4.

Claims 8, 9, 11, 17 and 18. Lee teaches that the display signal comprises first, second, and third color component signals, and the driver applies the initialization signal voltage and thereafter applies any one of the first, second, and third color component signals, to the display pixels connected to the scanning lines of the liquid crystal display panel, sequentially for every one of the scanning lines, in each of the signal application periods of the field period. Lee, col. 3, lines 40 – 53.

4. Claims 10 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al, in view of Moon as applied to claims 9 or 18 above, and further in view of Taira et al, USPN 6,825,823 B1.

Claims 10 and 19.

Neither Lee nor Moon specifically teach controlling the light emission color or the illumination light source.

Taira teaches controlling light emission color of an illumination light source, wherein the controlling of the light emission color includes controlling the light emission color of the light source so as to correspond to any of the first, second, and third color component signals that is applied to the display pixels in the applying of the display signal. Taira, col. 1, lines 6 – 11; and col. 2, lines 42 – 64.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the color scheme as taught by Taira with the liquid crystal display device and method as taught by Lee and Moon to provide sufficient response time to reduce color breakup interference. See Taira, col. 2, lines 28 – 41.

Response to Arguments

5. Applicant's arguments with respect to claims 1 - 19 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Matsubara et al., USPN 6,549,187 B1, teaches two gate pulses for a single pulse supplied to a signal line.

Yokoyama et al., USPN 6,590,522 B1, shows a gate voltage applied to the rise and the fall of a signal pulse.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leland R. Jorgensen whose telephone number is 571-272-7768. The examiner can normally be reached on Monday through Friday, 10:00 am through 6:00 pm..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on 571-272-3638. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

On July 15, 2005, the Central FAX Number will change to 571-273-8300. This new Central FAX Number is the result of relocating the Central FAX server to the Office's Alexandria, Virginia campus.

Most facsimile-transmitted patent application related correspondence is required to be sent to the Central FAX Number. To give customers time to adjust to the new Central FAX Number, faxes sent to the old number (703-872-9306) will be routed to the new number until September 15, 2005. After September 15, 2005, the old number will no longer be in service and 571-273-8300 will be the only facsimile number recognized for "centralized delivery".

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

lrj

KENT CHANG
PRIMARY EXAMINER